REMARKS

I. REAL PARTY IN INTEREST

The present Application was assigned to Altera Corporation, a Delaware corporation, as indicated by an assignment from the inventors recorded on February 12, 2004 in the Assignment Records of the United States Patent and Trademark Office at Reel 014970, Frame 0800.

II. RELATED APPEALS AND INTERFERENCES

Applicant, the undersigned Attorney, and Assignee are not aware of any related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in an appeal of this application.

III. STATUS OF CLAIMS

Claims 16, 18, 20-21, 23-24, 26-27, 33-35, and 37 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,867,727 ("Hattori") in view of U.S. Patent No. 5,557,750 ("Moore") and U.S. Patent No. 6,615,296 ("Daniel").

Claim 22 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hattori in view of Moore and Daniel and Patent Publication 2002/0152263 ("Gordrian").

Claims 38-51 are allowed.

IV. STATUS OF AMENDMENTS

This response after final is filed on September , 2007 in response to an Office Action made Final mailed June 4, 2007. No amendments to the claims have been made subsequent to the Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

With respect to independent claim 16 a method for managing data includes selecting a first first-in-first-out (FIFO) memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device (See p. 13 and Figure 4). The first data was prepared for output prior to a generation of the first read address from the data reading device (See p. 13-14 and Figures 4 and 5). The next data from a next storage element from the first FIFO memory is prepared for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device (See p. 8-9, and 13-14, and Figures 1-2, and 4-5).

With respect to independent claim 23 a method for managing data includes selecting a first first-in-first-out (FIFO) memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device (See p. 13 and Figure 4). The first data is output within a clock cycle after the first read address is generated (See p. 3 and 9, 13-14, and Figures 2 and 5). Next data from a next storage element from the first FIFO memory is prepared for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device (See p. 8-9, and 13-14, and Figures 1-2, and 4-5).

With respect to independent claim 33 a method for managing data includes selecting a first first-in-first-out (FIFO) memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device (See p. 13 and Figure 4). Next data from a next storage element from the first FIFO memory is prepared for output (See p. 8-9, and 13-14, and Figures 1-2, and 4-5). A second FIFO memory from the plurality of FIFO memories is selected to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device (See p. 13 and Figure 4). Next data from a next storage element from the second FIFO memory is prepared for output by transmitting a read

address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device (See p. 8-9, and 13-14, and Figures 1-2, and 4-5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Were claims 16, 18, 20-21, 23-24, 26-27, 33-35, and 37 properly rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,867,727 ("Hattori") in view of U.S. Patent No. 5,557,750 ("Moore") and U.S. Patent No. 6,615,296 ("Daniel")?

A. Does Hattori, Moore, and Daniel teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device?

B. Does Hattori, Moore, and Daniel teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data is output within a clock cycle after the first read address is generated?

VII. ARGUMENT 1

Claims 16, 18, 20-21, 23-24, 26-27, 33-35, and 37 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over as being unpatentable over U.S. Patent No. 5,867,727 ("Hattori") in view of U.S. Patent No. 5,557,750 ("Moore") and U.S. Patent No. 6,615,296 ("Daniel").

The Examiner has rejected claims 16, 18, 20-21, 23-24, 26-27, 33-35, and 37 as being unpatentable over Hattori, Moore, and Daniel.

It is submitted that Hattori, Moore, and Daniel do not render claims 16, 18, 20-21, 23-24, 26-27, 33-35, and 37, unpatentable under 35 U.S.C. §103(a).

Hattori includes a disclosure of data transferred via FIFO memories on a word unit basis. The FIFO memory is designated by an upper bit portion of a write address. An ID bit indicating whether a transfer word indicates a command or parameters is allocated to a lower bit portion and is written into the FIFO memory together with inherent word data. Upon reading, a lower bit portion of a read address is compared with the ID bit read out from the FIFO memory. When they don't coincide, the presence of an

error is decided. In case of adding redundant bits to the transfer word and judging a loss of word, on the transmission side, transmission side judgment bits having a fixed bit arrangement 01 of two bits are added to each word. Further, with respect to the m-th word, the transmission side judgment bits are shifted by (m-1) bits and a bit arrangement is changed and the resultant data is transmitted. On the reception side, the transmission side judgment bits are reversely shifted to the original positions and three bits in which one bit adjacent to the transmission side judgment bits was added thereto are checked. When a bit arrangement of the reception side judgment bits corresponding to the transmission side judgment bits coincides with a bit arrangement of the transmission side judgment bits, it is determined that there is no word loss. When they don't coincide, it is decided that there is a word loss (Hattori Abstract).

Moore includes a disclosure of a single chip peripheral bus adapter circuit has a pair of input and output first in, first out (FIFO) buffers, a main buffer, and a pair of supporting registers. The registers increase the performance of the circuit by eliminating or reducing wait states (Moore Abstract).

Daniel includes a disclosure of reducing FIFO access cycles across a system bus in a multi-processor system in which two processors communicate across a system bus through a FIFO, two separate FIFO descriptors are provided. The first descriptor is maintained by the processor located on-board with the FIFO, and the second descriptor is maintained by an off-board processor which communicates with the FIFO across the bus. When one processor performs a FIFO operation, the processor updates the other processor's descriptor via a memory access across the bus. Additionally, one module passes credits to the other to indicate that the latter has permission to perform a plurality of FIFO operations consecutively. In one embodiment a special non-valid data value is used to indicate an empty FIFO position (Daniel Abstract).

A. Applicants submit that Hattori, Moore, and Daniel do not teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device, and

preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

The Office Action mailed 6/4/2007 acknowledges that Hattori does not teach selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device (see 6/4/2007 Office Action, p. 3).

The Office Action mailed 6/4/2007 states in part that

> Moore teaches: "wherein the first data was prepared for output prior to a generation of the first read address from the data reading device;" (e.g., see column 7, lines 66-67 to column 8, lines 1-3; Fig. 2) For preparing the next data for prefetching within a clock cycle.
>
> Daniel teaches: "preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device ..." (e.g., see column 5, lines 63-64) For providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the net location within the FIFO to be read.

(6/4/2007 Office Action, p. 3).

Moore discloses a pre-fetch register 135 which lies between a host and a main FIFO 132. Data in this register 135 is fetched from the main FIFO 132 during available internal data bus cycles. This allows the data to be available when the host requests it. Applicant submits that the pre-fetch register 135 is operable to pre-fetch data from only a single FIFO such as main FIFO 132, not a plurality of FIFO memories as required by the claimed invention (Moore col. 1, line 67 through col. 2, line 7, col. 3, lines 54-62). Thus, Moore teaches away from selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device. Applicants submit that a prior art

reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, (Fed. Cir. 1983).

Daniel discloses providing an RD pointer that points to a next location within a FIFO to be read from. The RD pointer is maintained by an off-board processor which communicates with the FIFO across the bus (Daniel Abstract, col. 4, lines 40-49, and col. 6, lines 34-37). The RD pointer is a request for next data from a data reading device. Daniel does not disclose preparing next data for output prior to a request for the next data from the data reading device.

Furthermore, the techniques described in Daniel are also operable only with a single FIFO, not a plurality of FIFO memories as required by the claimed invention (Daniel Figures 3A-3F and 4A-4F). Thus, Daniel also teaches away from selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device.

In contrast, claim 16 states

> A method for managing data, comprising:
> selecting a first first-in-first-out (FIFO) memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device; and
> preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

(Claim 16) (Emphasis Added).

Claim 33 includes similar limitations. Given that claims 18, and 20-22 depend from claim 16, and claims 34-35, and 37 depend from claim 33 it is likewise submitted that claims 18, 20-22, 34-35, and 37 are also patentable under 35 U.S.C. §103(a) over Hattori, Moore, and Daniel.

B. Applicants submit that Hattori, Moore, and Daniel do not teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output within a clock cycle after the first read address is generated, and preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

The Office Action mailed 6/4/2007 acknowledges that Hattori does not teach selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data is output within a clock cycle after the first read address is generated (see 6/4/2007 Office Action, p. 5).

The Office Action mailed 6/4/2007 states in part that

> Moore teaches: "wherein the first data was prepared for output within a clock cycle after the first read address is generated;" (column 7, lines 23-24; and lines 66-67 to column 8, lines 1-4; Fig. 2).
> Daniel teaches: "preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device ..." (e.g., see column 5, lines 63-64) For providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the net location within the FIFO to be read.

(6/4/2007 Office Action, pp. 5-6).

Moore discloses a pre-fetch register 135 which lies between a host and a main FIFO 132. Data in this register 135 is fetched from the main FIFO 132 during available internal data bus cycles. This allows the data to be available when the host requests it. Applicant submits that the pre-fetch register 135 is operable to pre-fetch data from only a single FIFO such as main FIFO 132, not a plurality of FIFO memories as required by the claimed invention (Moore col. 1, line 67 through col. 2, line 7, col. 3, lines 54-62). Thus, Moore teaches away from selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a

first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device. Applicants submit that a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, (Fed. Cir. 1983).

Furthermore, Applicants submit that the text cited by the Office only discloses that "[o]n ACLK, the type of transfer for the next cycle is decided (this may be a prestore-to-FIFO transfer, a FIFO-to-prefetch transfer, a FIFO-to-peripheral interface transfer, or a peripheral interface-to-FIFO transfer)" (see Moore column 7, line 66 through column 8, line 3). The text cited by the Office does not disclose outputting first data within a clock cycle after the first read address is generated. In fact, the text cited makes no reference of outputting the first data or the read address generated for the first data.

Daniel discloses providing an RD pointer that points to a next location within a FIFO to be read from. The RD pointer is maintained by an off-board processor which communicates with the FIFO across the bus (Daniel Abstract, col. 4, lines 40-49, and col. 6, lines 34-37). The RD pointer is a request for next data from a data reading device. Daniel does not disclose preparing next data for output prior to a request for the next data from the data reading device nor does it disclose outputting data within a clock cycle after a read address for the data is generated.

Furthermore, the techniques described in Daniel are also operable only with a single FIFO, not a plurality of FIFO memories as required by the claimed invention (Daniel Figures 3A-3F and 4A-4F). Thus, Daniel also teaches away from selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device.

In contrast, claim 23 states

> A method for managing data, comprising:
> selecting a first first-in-first-out (FIFO) memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data is

output within a clock cycle after the first read address is generated; and

preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

(Claim 23) (Emphasis Added).

Given that claims 24, and 26-27 depend from claim 23, it is likewise submitted that claims 24, and 26-27 are also patentable under 35 U.S.C. §103(a) over Hattori, Moore, and Daniel.

In view of the arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-24 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicants' attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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